5

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,073	11/05/2003	Shiro Yoshioka	67471-029	6303

7590 01/03/2006

MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
GOGIA, ANKUR	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,073	YOSHIOKA ET AL.	
	Examiner	Art Unit	
	Ankur Gogia	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/701,073 has a total of 18 claims pending in the application; there are 4 independent claims and 14 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in the instant application.

Specification

4. The disclosure is objected to because of the following informalities: Page 21, line 18 and page 26, line 7 contain the word "cash" where it is believed the applicant intended to state "cache".

Furthermore, on page 55, line 16 it states "thorough the cache flush" where it is believed that the applicant intended to state "through the cache flush".

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 4 is rejected under 112, first paragraph, as failing to meet the written description requirement. The claim discloses wherein the access frequency index is updated such that a first value is added to the index when cache data has not been modified and a second value is added to the index when cache data has been modified. The instant specification of page 38 discloses wherein a value is added to the index. There does not appear to be any disclosure on how this value is obtained or whether it is different depending on the type of access.

8. Claims 6-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 6 discloses a management apparatus that performs wear leveling, however based on the examiner's understanding of wear leveling and the invention as disclosed, the examiner is unclear as to how the invention performs wear leveling. See the discussion in ¶s 19-21 below.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 2-10, 13, and 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 2 states the limitation "a degradation index" on lines 11 and 13, however claim 1 already provides "a degradation index" on line 17. It is unclear whether the degradation index of claim 2 is the same as or different from that of claim 1.

12. Claim 3 discloses wherein the degradation index updating unit adds **a sum of the first value and the second value** to a degradation index if the cache data has been modified, however claim 2, from which claim 3 depends, discloses wherein the degradation index updating unit is operable to add **a second value** to the degradation index if the cache data has been modified. These limitations appear to be contradictory in nature. Based on the description of the invention given and the examiners understanding of the disclosure as a whole the examination has been made under the assumption that the applicant intended for claim 3 to disclose that the second value is added to the index.

13. Claim 4 states the limitation "an access frequency index" on lines 4 and 7, however claim 1 already provides "an access frequency index" on line 12. It is unclear whether the access frequency index on claim 4 is the same as or different from that of claim 1.

14. Claim 5 discloses wherein the access frequency index updating unit adds **a sum of the first value and the second value** to an access frequency index if the cache data has been modified, however claim 4, from which claim 5 depends, discloses wherein the access frequency index updating unit is operable to add **a second value** to the access frequency index if the cache data has been modified. These limitations appear to be contradictory in nature. Based on the description of the invention given and the examiners understanding of the disclosure as a whole the examination has been made under the assumption that the applicant intended for claim 5 to disclose that the second value is added to the index.

15. Claim 6 discloses the limitation "a cache access frequency index" on line 8, however the claim already provides "a cache access frequency index" on line 3. It is unclear whether the cache access frequency on line 8 is the same as or different from that on line 3.

16. Claim 8 discloses the limitation "a cache access frequency index" on line 4, however claim 6 already provides "a cache access frequency index" on line 3. It is unclear whether the cache access frequency of claim 8 is the same as or different from that of claim 6. The claim also discloses the limitation "an access frequency index" on line 7, however claim 1 already provides "an access frequency index" on line 12. It is unclear whether the access frequency index of claim 8 is the same as or different from that of claim 1.

17. Claims 9, 13 and 16-18 all have deficiencies similar to claims 2, 4, 6 and 8 above. They all disclose a limitation of the form "a...index" that has already been

disclosed in an earlier parent claim. It is unclear whether the limitations of claims 9, 13 and 16-18 are the same as or different from that of the parent claims.

18. Any claims listed in ¶9 and not discussed specifically above, have been rejected for inheriting the deficiencies of the claims from which they depend.

Claim Rejections - 35 USC § 101

19. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

20. Claims 6-8 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility.

21. Claim 6 discloses an access frequency index updating unit operable to compare an access frequency index of a logical page mapped to a physical page with the cache access frequency index and updates the access frequency index with the cache access frequency index if the cache access frequency index is greater than the access frequency index.

The examiner interprets the invention as disclosed in claim 6 as follows. The apparatus disclosed performs wear leveling on an FeRAM such that a physical page that has a low degradation index is mapped to a logical page that has a high access frequency index, where the degradation index is an indication of the actual number of accesses to a physical page and the access frequency is an indication of the number of accesses to data in a cache, the data corresponding to data stored in the physical page **(Pg. 35, Lines 5-9)**.

Furthermore, the art recognized accepted meaning of wear leveling as is disclosed in the prior art is a technique for prolonging the life of certain kinds of erasable computer storage media such as flash memory and FeRAM. The method involves arranging the data so that erasures can be evenly distributed across the medium.

Based on the examiners interpretation of the invention and the art recognized meaning of wear leveling, the examiner is confused as to how the invention as disclosed in claim 6 performs wear leveling. As disclosed therein, the invention is using the factor of how often data is accessed in a cache as a basis for distributing wear in the FeRAM, however this would seem to not only not perform wear leveling but also result in excess wear as data will be moved more frequently than would be necessary. For example, an item of data may be accessed 1 time in physical memory and then 50 times in cache, while another item of data was accessed maybe 10 times in physical memory but only 20 times in cache. Assuming no other items have been accessed more frequently the first item would be moved, resulting in additional access to the physical memory at this location. However, the location of the second item would actually have more wear, since that physical location was accessed more.

Furthermore, it is disclosed that a heavily degraded physical page is mapped to a less frequently accessed logical page. The examiner is also confused as to how this would perform wear leveling. Based on the ordinary level of skill in the art, a logical page that is frequently accessed is done so due to the data that is stored in that page. By re-mapping the physical page to a logical page that is less accessed would not appear to reduce wear, since the data has not actually moved to a less accessed

portion of memory. Although the new logical page was previously less accessed, it would become more accessed after the mapping, since the data it maps to is highly accessed data. In other words, high access to a memory is due to the need for the data at the particular location, not because of the address of the location.

For the reasons above, the invention as disclosed in claim 6 appears to lack patentable utility.

Furthermore, claims 7-8 are rejected for inheriting the deficiencies of claim 6 from which they depend.

Claim Rejections - 35 USC § 102

22. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

23. Claims 1 and 15 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art (hereinafter referred to as AAPA).

Claim 1

AAPA discloses a memory management apparatus for accessing a physical page mapped according to mapping information to a logical page that includes a logical address specified by an access request, the mapping information showing a one-to-one mapping between a plurality of logical pages and a plurality of physical pages, the logical pages being defined by dividing a logical address space by a predetermined

size, each of the physical pages functioning to physically retain data of the predetermined size **(Pg. 2, Lines 1-23)** and degrading in storage performance each time an access is made thereto **(Pg. 1, Lines 16-23)**, the apparatus comprising:

an access frequency index storage unit operable to store an access frequency index for each logical page, the access frequency index indicating an occurrence frequency of an access request specifying a logical address included in a corresponding logical page **(Pg. 2, Lines 24-26; Pg. 3, Line 1)**;

a degradation index storage unit operable to store a degradation index for each physical page, the degradation index indicating a degree of degradation in storage performance of a corresponding physical page **(Pg. 2, Lines 24-26; Pg. 3, Line 3; It is noted that although the access frequency and degradation indices are disclosed as different indices, as disclosed they may in fact appear to be the same. The degradation index is disclosed as indicating a degree of degradation, however since an access results in degradation the access frequency would be a degree of degradation and therefore the indices as disclosed appear to track the same value (Pg. 37, Lines 24 – Pg. 38, Line 6))**; and

a degradation leveling unit operable to (i) exchange retained data between a first physical page and a second physical page, the first physical page being mapped according to the mapping information to a specific logical page of which an access frequency index is greater than or equal to a first threshold, and the second physical page having a degradation index that is less than or equal to a second threshold, and

(ii) update the mapping information so as to show that the specific logical page is mapped to the second physical page **(Pg. 2, Line 27 – Pg. 3, Line 12)**.

Claim 15

AAPA discloses a memory management method for accessing a physical page mapped according to mapping information to a logical page that includes a logical address specified by an access request, the mapping information showing a one-to-one mapping between a plurality of logical pages and a plurality of physical pages, the logical pages being defined by dividing a logical address space by a predetermined size, each of the physical pages functioning to physically retain data of the predetermined size **(Pg. 2, Lines 1-23)** and degrading in storage performance each time an access is made thereto **(Pg. 1, Lines 16-23)**, wherein

the method employs (i) an access frequency index indicating, for each logical page, an occurrence frequency of an access request specifying a logical address included in a corresponding logical page **(Pg. 2, Lines 24-26; Pg. 3, Line 1)** and (ii) a degradation index indicating, for each physical page, a degree of degradation in storage performance of a corresponding physical page **(Pg. 2, Lines 24-26; Pg. 3, Line 3; It is noted that although the access frequency and degradation indices are disclosed as different indices, as disclosed they may in fact appear to be the same. The degradation index is disclosed as indicating a degree of degradation, however since an access results in degradation the access frequency would be a degree of degradation and therefore the indices as disclosed appear to track the same value (Pg. 37, Lines 24 – Pg. 38, Line 6))**,

the method comprising:

a degradation leveling step of (i) exchanging retained data between a first physical page and a second physical page, the first physical page being mapped according to the mapping information to a specific logical page of which an access frequency index is greater than or equal to a first threshold, and the second physical page having a degradation index that is less than or equal to a second threshold, and (ii) updating the mapping information so as to show that the specific logical page is mapped to the second physical page **(Pg. 2, Line 27 – Pg. 3, Line 12)**.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 2-5, 9-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over AAPA in view of Bruce et al. (U.S. Pat. 6,000,006) and Coulson (U.S. PGPub 2003/0058681).

Claim 2

AAPA does not disclose expressly wherein the memory management apparatus further comprises:

a cache storage unit operable to store, for each of up to a predetermined number of the physical pages, cache data that is a copy of data retained in a corresponding

physical page and that is accessed instead of the original data, and to write, if cache data has been modified as a result of a subsequent access, the modified cache data back to a corresponding physical page; and

a degradation index updating unit operable to add a first value to a degradation index of each physical page that retains original data of cache data stored in the cache storage unit, and add a second value to a degradation index of each physical page to which modified cache data has been written back.

Bruce et al. disclose a method for wear leveling in a flash memory wherein frequently written data is stored in a cache and written back periodically **(Col. 5, Lines 22-24; Col. 6, Lines 22-31)**. They further disclose write counters that track the total number of writes to a physical block **(Col. 7, Lines 4-6)**. Since the write counters keep track of all writes to the physical memory, they would be incremented each time data from the cache is written back to the physical memory.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to incorporate a cache into a system for wear leveling.

The motivation for doing so would have been to extend the life of the memory **(Bruce et al. - Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 2.

The combination of AAPA and Bruce et al. does not disclose expressly, wherein the counter keeps track of reads as well as writes, however as is disclosed in Coulson, in a destructive read type memory such as FeRAM, the read consists of a write back operation **(¶22)**, therefore a read is inherently a write.

The combination of AAPA and Bruce et al. and Coulson are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of AAPA and Bruce et al. and Coulson before them, to track not only write access but read access in a read-destructive memory.

The motivation for doing so would have been leveling usage and reducing wear of memory devices **(Coulson - Abstract)**.

Therefore, it would have been obvious to combine Coulson with the combination of AAPA and Bruce et al. for the benefit of leveling usage and reducing wear of memory devices to obtain the invention as specified in claim 2.

Claim 3

AAPA does not disclose expressly wherein the degradation index updating unit adds, at a time when cache data is invalidated or replaced by data retained in another physical page, a sum of the first value and the second value to a degradation index of a

physical page storing original data of the cache data if the cache data has been modified, and adds the first value to the degradation index if the cache data has not been modified.

As discussed earlier, claim 3 is being interpreted such that a second value is added to the degradation index when cache data has been modified. Therefore, claim 3 is of the same scope as claim 2 and the discussion applied to claim 2 above also applies to claim 3. However, the discussion above does not mention that the degradation index is updated when the cache is invalidated. This limitation is inherent to the disclosure of Bruce et al. They disclose storing data in a cache and writing the data back at regular intervals and they further disclose tracking all writes to the physical data. When the cache is invalidated all data is updated to the memory and since at this point the data is written back to the physical memory the counter would keep track of these writes.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to incorporate a cache into a system for wear leveling and to track not only write access but read access in a read-destructive memory.

The motivation for doing so would have been to extend the life of the memory **(Bruce et al. - Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 3.

Claim 4

AAPA does not disclose expressly wherein the memory management apparatus further comprises:

an access frequency index updating unit operable to add a first value to an access frequency index of each physical page that retains original data of cache data stored in the cache storage unit, and add a second value to an access frequency index of each physical page to which modified cache data has been written back.

Bruce et al. disclose a method for wear leveling in a flash memory wherein frequently written data is stored in a cache and written back at certain time intervals **(Col. 5, Lines 22-24; Col. 6, Lines 22-31)**. They further disclose write counters that track the total number of writes to a physical block **(Col. 7, Lines 4-6)**.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to incorporate a cache into a system for wear leveling.

The motivation for doing so would have been to extend the life of the memory **(Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 4.

The combination of AAPA and Bruce et al. does not disclose expressly, wherein the counter keeps track of reads as well as writes, however as is disclosed in Coulson, in a destructive read type memory such as FeRAM, the read consists of a write back operation **(¶22)**, therefore a read is inherently a write.

The combination of AAPA and Bruce et al. and Coulson are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of AAPA and Bruce et al. and Coulson before them, to track not only write access but read access in a read-destructive memory.

The motivation for doing so would have been leveling usage and reducing wear of memory devices **(Coulson - Abstract)**.

Therefore, it would have been obvious to combine Coulson with the combination of AAPA and Bruce et al. for the benefit of leveling usage and reducing wear of memory devices to obtain the invention as specified in claim 4.

Claim 5

AAPA does not disclose expressly wherein the access frequency index updating unit adds, at a time when cache data is invalidated or replaced by data retained in another physical page, a sum of the first value and the second value to a access

frequency index of a physical page storing original data of the cache data if the cache data has been modified, and adds the first value to the access frequency index if the cache data has not been modified.

As discussed earlier, claim 5 is being interpreted as having intended to disclose adding a second value to the access frequency index when cache data has been modified. Therefore, claim 5 is of the same scope as claim 4 and the discussion applied to claim 4 above also applies to claim 5. However, the discussion above does not mention that the degradation index is updated when the cache is invalidated. This limitation is inherent to the disclosure of Bruce et al. They disclose storing data in a cache and writing the data back at regular intervals and they further disclose tracking all writes to the physical data. When the cache is invalidated all data is updated to the memory and since at this point the data is written back the counter would keep track of these writes.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to incorporate a cache into a system for wear leveling and to track not only write access but read access in a read-destructive memory.

The motivation for doing so would have been to extend the life of the memory **(Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 5.

Claim 9

AAPA further discloses wherein each logical page has a generic logical address that is included in a corresponding logical page,

the memory management apparatus further comprising:

a detecting unit operable to detect an access request specifying any of the generic logical addresses;

a degradation index updating unit operable to increment a degradation index of a physical page mapped according to the mapping information to a logical page that includes a generic logical address specified by an access request detected by the detecting unit; and

an access frequency index updating unit operable to increment an access frequency index of the logical page that includes the generic logical address specified by the detected access request **(Pg. 2, Lines 24-26)**.

Claim 10

AAPA further discloses wherein each generic logical address is a logical address that is accessed whenever a logical page including a corresponding generic logical address is accessed **(Pg. 2, Lines 5-12; In the reference, the data is accessed in blocks or pages, therefore the logical address of the page is the generic logical address.)**.

Claim 11

AAPA does not disclose expressly wherein each physical page is implemented by a ferroelectric random access memory.

Coulson discloses wherein data is stored in a ferroelectric memory **(¶16)**.

AAPA and Coulson are analogous art because they are from the similar problem solving area of wear leveling in a destructive memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Coulson before them, to use a ferroelectric random access memory to store data.

The motivation for doing so would have been inexpensive and higher yield manufacturing due to lack of transistors **(¶22)**.

Therefore, it would have been obvious to combine Coulson with AAPA for the benefit of inexpensive and higher yield manufacturing to obtain the invention as specified in claim 11.

Claim 16

AAPA does not disclose expressly the method further comprising:

a cache managing step of storing, for each of up to a predetermined number of the physical pages, cache data that is a copy of data retained in a corresponding physical page and that is accessed instead of the original data, and of writing, if cache data has been modified as a result of a subsequent access, the modified cache data back to a corresponding physical page; and

a degradation index updating step of adding a first value to a degradation index of each physical page that retains original data of cache data stored in the cache storage step, and adding a second value to a degradation index of each physical page to which modified cache data has been written back.

Bruce et al. disclose a method for wear leveling in a flash memory wherein frequently written data is stored in a cache and written back at certain time intervals **(Col. 5, Lines 22-24; Col. 6, Lines 22-31)**. They further disclose write counters that track the total number of writes to a physical block **(Col. 7, Lines 4-6)**. Although Bruce et al. do not explicitly disclose adding a first value for data that has not been modified and a second value for data that has been modified, it is inherent in their disclosure and in view of FTB. FTB discloses that a read operation for a FRAM requires a write operation, therefore a read is inherently a write. For this reason, when performing wear leveling on a memory that degrades with access, one of ordinary level in the art would recognize the need to add a first value for a read, which is inherently a write, and a second value for data that has been modified, since that encompasses a read and write back or inherently multiple writes.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to

incorporate a cache into a system for wear leveling and to track not only write access but read access in a read-destructive memory.

The motivation for doing so would have been to extend the life of the memory **(Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 16.

Claim 17

AAPA further discloses wherein

each logical page has a generic logical address that is included in a corresponding logical page,

the memory management method further comprising:

a detecting step of detecting an access request specifying any of the generic logical addresses;

a degradation index updating step of incrementing a degradation index of a physical page mapped according to the mapping information to a logical page that includes a generic logical address specified by an access request detected in the detecting step; and

an access frequency index updating step of incrementing an access frequency index of the logical page that includes the generic logical address specified by the detected access request **(Pg. 2, Lines 24-26)**.

26. Claims 12-13 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over AAPA in view of Bruce et al. and Bohrer et al. (U.S. PGPub 2004/0243761).

Claim 12

AAPA discloses a memory management apparatus for accessing a physical page mapped according to mapping information to a logical page that includes a logical address specified by an access request, the mapping information showing a one-to-one mapping between a plurality of logical pages and a plurality of physical pages, the logical pages being defined by dividing a logical address space by a predetermined size, each of the physical pages functioning to physically retain data of the predetermined size **(Pg. 2, Lines 1-23)** and degrading in storage performance each time an access is made thereto **(Pg. 1, Lines 16-23)**, the apparatus comprising:

an access frequency index storage unit operable to store an access frequency index for each logical page, the access frequency index indicating an occurrence frequency of an access request specifying a logical address included in a corresponding logical page **(Pg. 2, Lines 24-26; Pg. 3, Line 1)**;

AAPA does not disclose expressly the apparatus further comprising a cache storage unit operable to store cache data for each of up to a predetermined number of the physical pages in association with a replication access frequency index that is a copy of an access frequency index of a logical page mapped according to the mapping information to a corresponding physical page, the cache data being a copy of data retained in the corresponding physical page and that is accessed instead of the original data; and

a degradation leveling unit operable, when one of the pieces of cache data needs to be replaced with data retained in a new physical page, to replace cache data

associated with a replication access frequency index that is less than or equal to an access frequency index of a logical page mapped according to the mapping information to the new physical page.

Bruce et al. disclose a method for wear leveling in a flash memory wherein frequently written data is stored in a cache and written back periodically **(Col. 5, Lines 22-24; Col. 6, Lines 22-31)**.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to incorporate a cache into a system for wear leveling.

The motivation for doing so would have been to extend the life of the memory **(Bruce et al. - Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 12.

The combination of AAPA and Bruce et al. do not disclose expressly a cache entry replacement method wherein the entry with a low amount of hits is replaced.

Bohrer et al. disclose a method of managing storage of files on a multi-tiered disk system wherein a first disk is used similar to a cache and holds frequently accessed data while another disk holds less frequently accessed data **(Abstract)**. When data is to be transferred from the second tier to the first tier and an entry in the first tier needs to

be replaced due to lack of available space, the system determines the "popularity" of data in the first tier and replaces the least "popular" data, where the least "popular" data is data that has not been accessed lately **(¶14 and ¶22)**.

The combination of AAPA and Bruce et al. and Bohrer et al. are analogous art because they are from the similar problem solving area of improving performance in a cache memory system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of he combination of AAPA and Bruce et al. and Bohrer et al. before them, to incorporate an entry replacement method wherein an entry with a low amount of hits is replaced.

The motivation for doing so would have been to improve performance and reliability of storage devices **(¶5)**.

Therefore, it would have been obvious to combine Bohrer et al. with the combination of AAPA and Bruce et al. for the benefit of improved performance and reliability to obtain the invention as specified in claim 12.

Claim 13

The combination of AAPA and Bruce et al. does not disclose a replication access frequency index updating unit operable, in response to an access to cache data, to decrement a replication access frequency index associated with the cache data.

Bohrer et al. disclose in ¶14 keeping track of file statistics including an estimate access count of the file and using this information to determine the "popularity" of the file. By keeping track of the access, they must be either incrementing of decrementing

a counter. It is noted that whether they increment or decrement the count, they are still tracking access frequency and therefore the result will be the same

The combination of AAPA and Bruce et al. and Bohrer et al. are analogous art because they are from the similar problem solving area of improving performance in a cache memory system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of he combination of AAPA and Bruce et al. and Bohrer et al. before them, to incorporate an entry replacement method wherein an entry with a low amount of hits is replaced.

The motivation for doing so would have been to improve performance and reliability of storage devices **(¶5)**.

Therefore, it would have been obvious to combine Bohrer et al. with the combination of AAPA and Bruce et al. for the benefit of improved performance and reliability to obtain the invention as specified in claim 13.

Claim 18

AAPA discloses a memory management method for accessing a physical page mapped according to mapping information to a logical page that includes a logical address specified by an access request, the mapping information showing a one-to-one mapping between a plurality of logical pages and a plurality of physical pages, the logical pages being defined by dividing a logical address space by a predetermined size, each of the physical pages functioning to physically retain data of the

predetermined size **(Pg. 2, Lines 1-23)** and degrading in storage performance each time an access is made thereto **(Pg. 1, Lines 16-23)**, wherein

the method employs (i) an access frequency index indicating, for each logical page, an occurrence frequency of an access request specifying a logical address included in a corresponding logical page **(Pg. 2, Lines 24-26; Pg. 3, Line 1)** and (ii) a degradation index indicating, for each physical page, a degree of degradation in storage performance of a corresponding physical page **(Pg. 2, Lines 24-26; Pg. 3, Line 3)**,

AAPA does not disclose expressly the method comprising:

a cache storing step of storing cache data for each of up to a predetermined number of the physical pages in association with a replication access frequency index that is a copy of an access frequency index of a logical page mapped according to the mapping information to a corresponding physical page, the cache data being a copy of data retained in the corresponding physical page and that is accessed instead of the original data; and

a degradation leveling step of, when one of the pieces of cache data needs to be replaced with data retained in a new physical page, replacing cache data associated with a replication access frequency index that is less than or equal to an access frequency index of a logical page mapped according to the mapping information to the new physical page.

Bruce et al. disclose a method for wear leveling in a flash memory wherein frequently written data is stored in a cache and written back periodically **(Col. 5, Lines 22-24; Col. 6, Lines 22-31)**.

AAPA and Bruce et al. are analogous art because they are from the similar problem solving area of wear leveling in a memory that degrades with increased access.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Bruce et al. before them, to incorporate a cache into a system for wear leveling.

The motivation for doing so would have been to extend the life of the memory **(Bruce et al. - Col. 5, Lines 24-26)**.

Therefore, it would have been obvious to combine Bruce et al. with AAPA for the benefit of extended memory life to obtain the invention as specified in claim 18.

The combination of AAPA and Bruce et al. do not disclose expressly a cache entry replacement method wherein the entry with a low amount of hits is replaced.

Bohrer et al. disclose a method of managing storage of files on a multi-tiered disk system wherein a first disk is used similar to a cache and holds frequently accessed data while another disk holds less frequently accessed data **(Abstract)**. When data is to be transferred from the second tier to the first tier and an entry in the first tier needs to be replaced due to lack of available space, the system determines the "popularity" of data in the first tier and replaces the least "popular" data, where the least "popular" data is data that has not been accessed lately **(¶14 and ¶22)**.

The combination of AAPA and Bruce et al. and Bohrer et al. are analogous art because they are from the similar problem solving area of improving performance in a cache memory system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of he combination of AAPA and Bruce et al. and Bohrer et al. before them, to incorporate an entry replacement method wherein an entry with a low amount of hits is replaced.

The motivation for doing so would have been to improve performance and reliability of storage devices **(¶5)**.

Therefore, it would have been obvious to combine Bohrer et al. with the combination of AAPA and Bruce et al. for the benefit of improved performance and reliability to obtain the invention as specified in claim 18.

27. Claim 14 is rejected under 35 U.S.C. 103(a) as being obvious over AAPA in view of Bruce et al. and Bohrer et al. as applied to claim 12 above and further in view of Coulson.

Claim 14

The combination of AAPA, Bruce et al. and Bohrer et al. does not disclose expressly wherein each physical page is implemented by a ferroelectric random access memory.

Coulson discloses wherein data is stored in a ferroelectric memory **(¶16)**.

The combination of AAPA, Bruce et al. and Bohrer et al. and Coulson are analogous art because they are from the similar problem solving area of wear leveling in a destructive memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of AAPA, Bruce et al. and Bohrer

et al. and Coulson before them, to use a ferroelectric random access memory to store data.

The motivation for doing so would have been inexpensive and higher yield manufacturing due to lack of transistors **(¶22)**.

Therefore, it would have been obvious to combine Coulson with the combination of AAPA, Bruce et al. and Bohrer et al. for the benefit of inexpensive and higher yield manufacturing to obtain the invention as specified in claim 14.

28. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See M.P.E.P. 707.05(c).

Relevant Art Cited by Examiner

29. The following references teach various wear leveling techniques.

U.S. Patent/Pub. Number	**Relevant Sections**
2003/0163633	
6,957,158	Col. 10, Line 39-Col. 11, Line 15
5,602,987	Abstract
5,930,193	
5,737,742	

Non-Patent Literature	**Relevant Sections**
"FRAM Technology Backgrounder"	

Conclusion

30. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a first action non-final.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankur Gogia whose telephone number is 571-272-4166. The examiner can normally be reached on M-F 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. M.

Ankur Gogia
Examiner
Art Unit 2187

12/22/2005

C. P. C.

CHRISTIAN CHACE
PRIMARY EXAMINER